IN THE SPECIFICATION

Amend paragraph 4 as follows:

Another essential feature of image fidelity is the isolation of image information to the ~~intended area, region, or~~ display elements addressed by the addressing means. Capacitive coupling between, and resistive losses in, array bus electrodes conducting electrical signals from the addressing means to the display elements is a contributing factor to degradation of image fidelity by unintended transference of image information to non-addressed display elements and reduction of addressing signal amplitude to addressed ~~between the~~ display elements.

Amend paragraph 9 as follows:

A variation of the pin-matrix system contained a multilayer dielectric mirror suspended over the non-vacuum side of a pin-matrix faceplate. The mirror was deformed at the conductive pins in response to charge deposited by an electron beam. This device functioned optically in a manner similar to that employed in the currently commercially successful Texas Instruments DLP projectors. U.S. Patents 5,287,215 and 5,471,341 ~~5,471,314~~ describe a more modern embodiment of this concept.

Amend paragraph 11 as follows:

An electron-beam-addressed liquid-crystal display developed by Tektronix utilized electron-beam-induced secondary electron emission from a dielectric surface to produce a localized positive charge on a thin dielectric membrane that separated a liquid-crystal film from the vacuum environment. The liquid-crystal film was divided into an array of liquid-crystal cells. Responsive ~~Responding~~ to the electric field induced by the deposited charge, the liquid-crystal cells modulated polarized light to create a projected image. The charge pattern created by a "writing" electron beam remained on the dielectric membrane until removed by an "erase" electron beam.

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Amend paragraph 13 as follows:

In each case of recent prior art ~~art,~~ where the addressing technique utilizes charge deposition by an electron beam and where the display technique employs liquid-crystal modulation resulting from the deposited charge, the mechanism used to transfer information (electrical signals) from the electron-beam target to the display electrodes of the liquid crystal cells has fundamentally limited the resolution of the display. Additionally, the liquid crystal must be isolated from the vacuum environment required for generation of the electron beam.

Amend paragraph 25 as follows:

The benefits of the present active-matrix light modulator can be seen by examining how the transistors and liquid-crystal cells are operated in accordance with the invention to assist in presenting an image. Starting with all the transistors in their non-conductive conditions, selected ones of the transistors are sequentially bombarded with electrons according to an image pattern at a dosage and average energy that cause each selected transistor to enter its conductive condition. During the sequential electron bombardment of the selected transistors, all of the transistors are disabled. Accordingly, the selected transistors do not yet conduct current even though they are in their conductive conditions. The liquid-crystal cells do not yet start to assist in presenting an image corresponding to the image pattern. The sequential electron bombardment is preferably done with a scanning electron beam of the electron-beam system.

Amend paragraph 26 as follows:

Each selected transistor is subsequently enabled in a writing manner that results in the polarization direction of the specified light being selectively rotated in the corresponding liquid-crystal cell. When there are multiple selected transistors, all of the selected transistors are enabled substantially simultaneously in the writing manner. This results in the polarization directions of the specified light being selectively rotated substantially simultaneously in all of the liquid-crystal cells corresponding to the selected transistors. Using a suitably located polarization analyzer, the combination of the liquid-crystal cells,

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substrate, and polarization analyzer thereby presents ~~present~~ the entire image at substantially the same instant. Operating in this manner enables the active-matrix light modulator of the invention to avoid undesirable time-varying image artifacts.

Amend paragraph 48 as follows:

Referring to the drawings, FIGs. 1a and 1b (collectively "FIG. 1") together illustrate a reflective liquid-crystal light modulator in accordance with the invention. The light modulator of FIG. 1 includes a thin flexible membrane 200, an active matrix 201 disposed along one side (the upper side in FIG. 1a) of membrane 200, a two-dimensional array of display electrodes 31 disposed along the other side (the lower side in FIG. 1a) of membrane 200, electrically conductive means 49 for electrical communication between active matrix 201 and display electrodes 31, a layer 70 of liquid crystal divided into a two-dimensional array of liquid-crystal cells 202 respectively corresponding to display electrodes 31, an electrically insulating transparent modulator substrate 90, a common transparent electrode 91 situated on substrate 90, a control component 203, and an electron-beam system formed with a writing electron gun 400 and an erasing electron gun 500. Writing electron gun 400 generates a scanning electron beam 401 for addressing active matrix 201. Erase electron gun 500 generates an electron beam 501 for use in flood erasing matrix 201.

Amend paragraph 54 as follows:

More particularly, the light-modulator structure of FIG. 1 is allocated into a two-dimensional ~~an~~ array of ~~or~~ rows and columns of pixels as indicated in FIG. 2. The subpixels in each pixel are similarly arranged in a two-dimensional subarray of rows and columns. The subpixels have an average subpixel width in a first lateral direction, e.g., the vertical direction in FIG. 2. The average subpixel width in the first lateral direction is typically the average width of TFTs 204, specifically their gate elements (described further below), in the first lateral direction.

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Amend paragraph 55 as follows:

As described below, electron beam 401 of writing electron gun 401 scans TFTs 204 during transistor writing operations. In scanning TFTs 204 in a second lateral direction, e.g., the horizontal direction in FIG. 2, generally perpendicular to the first lateral direction, beam 401 has a beam width in the first lateral direction. As indicated below in connection with FIG. 4, beam 401 provides electrons having a generally Gaussian spatial distribution perpendicular to the direction of beam travel. Based on this Gaussian electron distribution, the beam width is the Gaussian distribution width at which the electron current density in beam 401 is one half (50%) of the maximum electron current density in beam 401. The Gaussian-shaped curve at the right-hand side of FIG. 2 indicates the Gaussian electron distribution as beam 401 moves in the second lateral direction, the horizontal direction in FIG. 2, over TFTs 204.

Amend paragraph 56 as follows:

The beam width is normally approximately, at least, the average pixel width in the first lateral direction and, in the case of FIG. 2 where each pixel has two subpixels in line with each other in the first lateral direction, twice the average subpixel width in the first lateral direction. Twice the subpixel width is defined as the lateral dimension between the centers of the two transistor gate elements (pitch) in a lateral direction plus the lateral width dimension of the transistor gate element in the same lateral direction. ~~dimension.~~ When the transistor gate-element dimension is not the same for the first and second lateral directions, the average pixel width is the greater of the two dimensions. For the more general case in which a pixel contains two or more subpixels in line with one another in the first lateral direction, the beam width is at least twice the pixel width. Where a pixel contains three or more subpixels in line with one another in the first lateral direction, the beam width is not less than three times the average subpixel width. Hence beam 401 scans along a line whose width is at least twice the average subpixel width and thus at least twice the average transistor width.

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Between paragraphs 56 and 57, insert the following new paragraph:

Distortion of a continuous line due to the nature of a screen display is termed aliasing. Taking note of the fact that anti-aliasing consists of smoothening rough, jagged edges of curved and diagonal lines as specified in Sol et al., "Anti-alias", Web Developer's™ Virtual Library, 1 April 1998, p. 1, the use of subpixels in the light modulator of Fig. 1 combined with scanning the subpixels in the foregoing manner provides anti-aliasing.

Amend paragraph 59 as follows:

Data information is applied to the gate element of each TFT 204 in order to vary the source-drain current I_{SD} through that TFT 204. ~~204 as shown in FIG. 2.~~ Source-drain current (or simply source current) I_{SD} is a function of gate voltage V_D as shown in FIG. 4. ~~V_D.~~ For typical TFT geometry, there is a region in which source current I_{SD} varies fairly linearly (on a logarithmic scale) with gate voltage V_G. The operating TFT range is the gate-voltage range between the threshold voltage V_{th} at which TFTs 204 turn on (start to conduct current) and the voltage V_{sat} at which TFTs 204 saturate.

Amend paragraph 75 as follows:

The light modulator of FIG. 1 operates in a reflective mode with display electrodes 31 being light reflective at least along their flat liquid-crystal-contacting surfaces (lower surfaces in FIG. 1a). Double-headed arrow 912 in FIG. 1a indicates linearly polarized visible light that impinges on the front surface (lower surface in FIG. 1a) of substrate 90 at the front of the light modulator, passes through substrate 90 and common electrode 91, passes through a liquid-crystal cell 202 where the light's polarization direction may undergo rotation depending on liquid-crystal voltage V_{LC} (not indicated in FIG. 1a) across that cell 202, is reflected off the liquid-crystal-contacting surface of corresponding display electrode 31, passes back through that cell 202 where the light's polarization direction may undergo further rotation, and passes back through common electrode 91 and substrate 90 and out the front of the light modulator.

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Amend paragraph 78 as follows:

A storage capacitor C_S is formed with each display electrode 31, the overlying part of a storage capacitor dielectric layer 41 of insulating polymer, and the further overlying part of ground plane 44 as also shown in FIG. 1a. Each storage capacitor C_S corresponds to, and is connected electrically in parallel with, one of liquid-crystal capacitors C_{LC}. Storage capacitors C_S provides additional storage capacity for liquid-crystal capacitors C_{LC} so that minor charge leakage from cell capacitors C_{LC}, caused by possible fabrication defects, is compensated for by reserve charge in storage capacitors C_S. This ensures that desired image gray level is maintained.

Amend paragraph 81 as follows:

Membrane 200, which isolates liquid-crystal cells 202 from the high-vacuum electron beam environment, consists of ~~of a~~ lower dielectric layer 41 of insulating polymer disposed over display electrodes 31, conductive ~~a conductive~~ ground plane 44 overlying lower ~~insulating~~ polymer dielectric layer 41, and an upper dielectric layer 45 of insulating polymer ~~polymer 45~~ overlying ground plane 44. Ground plane 44 is typically connected in common with common electrode 91 to line 441 for receiving common-plane reference voltage V_{ref}. The thickness of membrane 200 is typically less than 3 μm to provide sufficient flexibility to conform to deviations in the surface flatness of transparent substrate 90, with sufficient strength and durability due to multilayer construction to withstand cell processing and handling without loss of mechanical integrity. Molded spacers 43 formed in lower ~~insulating~~ polymer dielectric layer 41 precisely control the thickness of liquid-crystal layer 70 disposed between light-reflective display electrodes 31 and ITO-coated glass faceplate 90.

Amend paragraph 84 as follows:

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During a first time interval constituting a subset of the time required for a video field, reference potential V_{ref} is set to 0 V. Collector potential V_{coll} is set to 10 V relative to reference potential V_{ref} to provide a high collection field at 10 V/μm. Erase gun electron beam 501 is off. Writing gun cathode potential V_{wgk} is set at -200 V with respect to reference voltage V_{ref}. Average electron energy V_{PE} of writing beam 401 is greater than first electron

crossover potential V_{CR1}, and delta layer 59 of each selected TFT 204 charges in the positive direction toward collector potential V_{coll}. With the distribution of electron current I_{wb} in scanning electron beam of writing electron gun 400 being substantially Gaussian as shown in FIG. 2, ~~FIG. 4,~~ beam 401 sequentially scans each horizontal line in the TFT array and induces positive charge on delta coating 59 of each selected TFT 204 by means of secondary electron emission as shown in FIG. 4. ~~FIG. 3. Delta coating 59 of each selected TFT 204 charges (+) toward adjacently located collector potential V_{coll}.~~ The magnitude of the induced positive charge (δ-charge) is proportional to electron current I_{wb} in writing electron beam 401 and the dwell time of beam 401. The magnitude of electron-beam current I_{wb} is determined by the input picture information. The electron-beam dwell time on any TFT 204 is inversely proportional to the number of pixels in the display, but is constant for any specific resolution, e.g., less than 1.5 nsec for a 2500-line display.

Amend paragraph 85 as follows

Each delta coating 59 remains charged to the writing potential, i.e., less than or equal to collector voltage V_{coll}, ~~written potential~~ until the deposited charge is erased by aerial electrons since there is no conducting discharge path. During this first time interval, voltage V_D on drain electrodes 54 is set to high-impedance off potential V_{HZ}. Although there is a charge-induced electric field on the TFT channel regions causing TFTs 204 to be in their conductive conditions, ~~regions,~~ there is no source current to charge liquid-crystal cell capacitors C_{LC} and storage capacitors C_S. Consequently, no image is displayed as the entire video field is written into TFTs 204.

Amend paragraph 86 as follows:

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During a second time interval constituting a subset of the time required for the video field, after the entire TFT array is written, with the charge pattern representing a field of video information stored on delta coatings 59 in the TFT array, a short positive voltage pulse is applied to drain electrodes 54 of all TFTs 204 in the array. That is, drain voltage V_D is switched to value V_{CW+}, typically 5 V, to provide voltage V_{CW+} to all of the electrodes 54.

Source-drain current I_{SD} charges each selected liquid-crystal capacitor C_{LC} formed with a selected liquid-crystal cell 202, corresponding display electrode 31, and the underlying part of cell common electrode 91. Source current I_{SD} also charges corresponding storage capacitor C_s formed in parallel to cell capacitor C_{LC} by that display electrode 31, the overlying part of dielectric layer 41, and the further overlying part of ground plane 44. The duration of the V_D pulse is determined by the time required to charge capacitors C_{LC} and C_s to maximum with maximum gate voltage V_G. A typical V_D pulse width is 1 msec.

Amend paragraph 92 as follows:

The polarity of drain voltage V_D during TFT writing operations (second ~~(first~~ interval) is inverted (switched between V_{cw+} and V_{cw-}) on alternate video fields. This prevents DC offset at liquid-crystal cells 202.

Amend paragraph 95 as follows:

FIGs. 6a - 6e (collectively "FIG. 6") illustrate steps in accordance with the invention for manufacturing a mandrel substrate on which the light modulator of FIG 1a ~~FIG. 6~~ is fabricated. Referring to FIG. 6a, the starting material is substrate ~~material~~ 10 preferably consisting of glass such as Corning 1737 or equivalent at a thickness of 0.7 - 1.1 mm in ~~μm. In~~ order to be compatible with existing active matrix array commercial tools and processes. A ~~processes, a~~ blanket layer 11 of nickel is deposited by sputtering means to a thickness of 1.3 μm. The nickel-layer thickness is defined according to calculations describing the desired optical thickness of liquid-crystal layer 70. Nickel layer 11 is polished by chemical mechanical polishing (or planarization) to a high reflectivity.

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Amend paragraph 96 as follows:

Nickel layer 11 is coated with a positive tone photoresist 100 typically provided by Arch Chemical Company or other commercial vendor. Photoresist 100 is exposed to actinic light through a photomask and developed by conventional means to define a pattern

102 in ~~the~~ resist 100 whereby portions of nickel layer 11 are uncovered. The uncovered portions of nickel layer 11 are chemically etched in a commercially available etchant provided by Transene Chemicals or other vendor to remove nickel metal in the regions defined by pattern 102, thereby producing a nickel spacer mold 21 ~~102~~ as shown in FIG. 6b. Glass substrate 10 is not chemically attacked by the etchant. ~~etching process.~~ A tapering cross section for ~~of~~ spacer mold 21 is created by addition of 1.5 volume percent nitric acid to the nickel etchant.

FIG. 6c ~~FIG. 6c.~~ shows mandrel 20, including spacer mold 21, after removal of photoresist 100 by conventional chemical means. The diameter of spacer mold 21 is typically 1.5 μm. The depth of spacer mold 21 is controlled by the thickness of nickel layer 11 since substrate 10 is not attacked by the nickel pattern etchant ~~etching process.~~ FIG. 6d shows a plan view of mandrel 20. Spacer mold 21 is disposed in a regular array for which the preferred dimension between the centers of the features of spacer mold ~~feature~~ 21 in the x-direction is 5 μm, and the preferred dimension between the mold-feature centers in the y-direction is 5 μm. Mandrel 20, including spacer mold 21 and substrate 10 exposed at the bottom of spacer mold 21, is coated with a mold release 22 by sputtering means as shown in FIG. 6e. The preferred material for mold release 22 is a material containing amorphous carbon or boron carbide.

Amend paragraph 97 as follows:

FIGs. 7a - 7j (collectively "FIG. 7") illustrate initial steps in accordance with the invention for manufacturing the light modulator of FIG. 1a using mandrel substrate 20 fabricated according to process of FIG. 6. FIG. 7 specifically shows a preferred process sequence for fabrication of a flexible conformal film, incorporating an array of TFTs ~~transistors~~ disposed on a first side, and a corresponding array of display electrodes disposed on a second side. In FIG. 7a, a layer 30 of aluminum ~~aluminum 30~~ is deposited over mandrel 20 to a preferred thickness of 1 μm by sputtering means, and is coated with a positive tone photoresist 100. Photoresist 100 is exposed to actinic light through a photomask, with alignment and optical registration, ~~registration~~ to superimpose a pattern 103 on ~~to~~ previously defined pattern 102 as shown in FIG. 7b, and developed by conventional means to define a

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pattern 103 in resist 100 whereby portions of aluminum layer 30 are uncovered. Fig 7c is a plan view of photopattern 103.

The uncovered portions of aluminum layer 30 are chemically etched with a commercially available etchant provided by Transene Chemicals or other vendor to remove aluminum metal in the regions defined by pattern 103 to define display electrodes 31 as shown in FIG. 7d. Mold release 22 is not chemically attacked by the aluminum etchant. Display electrodes 31 are disposed in a regular array over mandrel 20 as shown in FIG. 7e, a plan view of display electrodes 31 disposed on mandrel 20, where the preferred dimension between the centers of display electrodes 31 in the x-direction is 5 μm, and the preferred dimension between the display-electrode centers in the y-direction is 5 μm. Photoresist 100 having pattern 103 is removed.

Amend paragraph 98 as follows:

Mandrel 20, together with the display electrode array and spacer mold 21, is coated with a liquid polymer material, such as PI 2610 supplied by HD Microsystems, and cured at 350°C to a preferred film thickness of 0.5 - 1 μm to form display element storage capacitor dielectric layer 41 and ~~41, and~~ spacer elements 43. The polymer of dielectric layer ~~43 as shown in FIG. 4b. Polymer~~ 41 adheres to display electrodes 31, but does not adhere to mold release 22. A layer 42 of chromium is deposited by sputtering ~~sputter~~ means over capacitor dielectric 41 to a film thickness of 100 nm as shown in FIG. 7f.

Chromium layer 42 is coated with a positive tone photoresist 100 and exposed to actinic light through a photomask, with alignment and optical registration, ~~registration~~ to superimpose a pattern 104 on ~~to~~ previously defined pattern 103. Photoresist 100 is ~~103 as shown in FIG. 7g, and~~ developed by conventional means to define pattern ~~a pattern~~ 104 in resist 100 whereby portions of chromium layer 42 are uncovered as shown in FIG. 7g. ~~uncovered.~~ The uncovered chromium is chemically etched with a commercially available etchant provided by Transene Chemicals or other vendor to remove the chromium metal in the regions defined by pattern 104 to define ground plane 44 as shown in FIG. 7h. Photoresist 100 having pattern 104 is removed.

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A second layer of liquid polymer material, such as PI 2610 supplied by HD Microsystems, is coated over ground plane 44 and the exposed portions of storage capacitor dielectric 41, and cured at 350°C to a preferred film thickness range of 0.5 - 1 μm to form first isolation dielectric layer 45 as shown in FIG. 7i. Second ~~A second~~ isolation dielectric layer 46 of passivating electrically insulating material is deposited over first isolation dielectric layer 45 to a preferred thickness of 200 nm as shown in FIG. 7j. The preferred material for dielectric layer 46 is silicon dioxide deposited by a plasma enhanced chemical vapor deposition ("PECVD") process.

Amend paragraph 99 as follows:

FIGs. 8a - 8m (collectively "FIG. 8") illustrate further steps in accordance with the invention for manufacturing the light modulator of FIG. 1a ~~FIG. 1~~ starting with the intermediate structure fabricated according to the steps of FIG. 7. FIG. 8 presents a preferred sequence for fabrication of the TFT array. A blanket layer 47 of amorphous silicon (α-Si) is ~~47 is~~ deposited by conventional PECVD means from a gaseous mix of silane and helium to a preferred thickness of 90 nm as shown in FIG. 8a. Blanket amorphous silicon layer 47 is then made conductive to contact with metals forming silicides. A preferred metal is chromium. Referring to FIG. 8b, silicon layer 47 is made electrically conductive n-type by bombarding it with phosphorus ions at an energy of 30 kV and a high dosage of 4×10^{15} ions/cm^2.

Amend paragraph 100 as follows:

As shown in FIG. 8c, heavily doped n-type silicon layer 47 is coated with a positive tone photoresist 100 and exposed to actinic light through a photomask, with alignment and optical registration, ~~registration~~ to superimpose a pattern 105 on ~~to~~ the previously defined array of display electrodes 31. Photoresist 100 is ~~electrodes 31, and~~ subsequently developed by conventional means to define pattern 105 in ~~the~~ resist 100 whereby portions of amorphous silicon layer 47 are uncovered. The uncovered portions of silicon layer 47 are etched by conventional reactive ion etching ("RIE") in a gas containing fluoride ions to define an array

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of heavily doped n-type source/drain pairs 48 as shown in FIG. 8d. A preferred etching gas is sulfur hexafluoride (SF_6). Photoresist 100 having pattern 105 is removed.

Each source/drain pair 48 is associated with, and overlies, a display electrode location. In each source/drain pair 48, ~~pair,~~ a first region 51, associated with a source electrode, and a second region 52, associated with a drain electrode, are spaced apart by a distance determined by the requirements for TFT channel geometry. In the present invention, the channel length is 2 μm, and the channel width is 3 μm. Additionally, each source/drain region 51 or 52 is comprised of a first contact area CA1 and a second contact area CA2. Contact area CA1 constitutes approximately half of the area of region 51 or 52. Contact area CA2 constitutes the remaining half.

Amend paragraph 101 as follows:

As shown in FIG. 8e, second dielectric layer 46, together with the array of source/drain pairs ~~pair array~~ 48, is coated with a positive tone photoresist 100 and exposed to actinic light through a photomask, with alignment and optical registration, ~~registration~~ to superimpose a source via pattern 106 on ~~to~~ the previously defined display electrode array. Photoresist 100 is ~~array, and~~ subsequently developed by conventional means to define pattern 106 in resist 100 whereby portions of second ~~dielectric~~ isolation dielectric layer 46 are uncovered. The exposed material of layer 46 is etched by conventional RIE gas chemistry containing fluoride ions to expose portions of first isolation dielectric layer 45. A preferred RIE gas composition is sulfur hexafluoride.

Isolation dielectric layer 45, together with storage capacitor dielectric layer 41, is dry etched by conventional oxygen plasma gas chemistry to form source vias 49. Display electrodes 31 are not etched by the chemistry used to etch source vias 49, and so provide ~~provides~~ a stop for the etching process. Vias 49 are subsequently etched by wet chemistry containing fluoride ions to remove residues from the dry etch process and to etch back second isolation dielectric layer 46 to increase the via dimension in layer 46 as shown in FIG. 8f to a larger dimension than source vias 49 in layer 45. Photoresist 100 having pattern 106 is removed.

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Amend paragraph 102 as follows:

A blanket layer 50 of metal ~~metal 50~~ forming ohmic contact to n+ source/drain pairs ~~pair array~~ 48 is deposited by sputtering means over second isolation dielectric layer 46, over source/drain pairs ~~pair array~~ 48 and into source vias 49 to contact ~~49, contacting~~ the exposed portions of display electrodes 31. A preferred metal is chromium deposited to a thickness of 200 nm. As shown in FIG. 8g, metal layer 50 is coated with a positive tone photoresist 100 and exposed to actinic light through a photomask, with alignment and optical registration, ~~registration~~ to superimpose a pattern 107 over previously defined source/drain pairs 48. Photoresist 100 is ~~pairs 48, and~~ subsequently developed by conventional means to define pattern 107 in resist 100 whereby portions of metal layer 50 are uncovered. The uncovered portions of layer 50 are chemically etched with a commercially available etchant provided by Transene Chemicals or other vendor to remove the metal in the regions defined by pattern 107 to define source-electrode pattern 53 and drain-electrode pattern 54.

Each source electrode 53 overlies a source via 49, making electrical contact to a display electrode 31, and associated ~~an associated~~ contact area CA1 of a source region 51 as shown in FIG. 8h. Each drain electrode 54 is electrically connected in common to all other drain electrodes 54 and makes electrical contact to associated contact area CA1 of a drain region 52. Photoresist 100 having pattern 107 is removed.

Amend paragraph 103 as follows:

A semiconductor layer 55 of amorphous silicon (α-Si) is deposited by conventional PECVD means from a gaseous mix of silane and helium to a preferred thickness of 90 nm so as to overlie the array of source/drain pairs ~~pair array~~ 48, source electrodes 53, drain electrodes 54, and second isolation dielectric 46. A gate dielectric layer 56 of silicon nitride is deposited by PECVD from a gas mix of silane and ammonia over silicon layer 55. Layers 55 and 56 are preferably deposited sequentially from the same deposition tool without exposure of amorphous silicon layer 55 to atmospheric contamination.

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Gate dielectric layer 56 is coated with a positive tone photoresist 100 and exposed to actinic light through a photomask, with alignment and optical registration, ~~registration~~ to superimpose a pattern 108 over the previously defined array of source/drain pairs 48. Photoresist 100 is ~~pair array 48, and~~ subsequently developed by conventional means to define pattern 108 in resist 100 whereby portions of gate dielectric layer 56 are uncovered. The exposed portions of gate dielectric layer 56 and silicon layer 55 are sequentially dry etched by conventional RIE means using sulfur hexafluoride gas chemistry to define silicon islands 57 together with overlying gate dielectric layers 58. Source electrodes 53 and drain electrodes ~~electrode~~ 54 are not etched by this chemistry, and so provide etch stopping. Photoresist 100 having pattern 108 is removed. Each silicon island 57 overlies the contact area CA2 of a source region 51 and contact area CA2 of associated drain region 52 as shown in FIG. 8i.

Amend paragraph 104 as follows:

Referring to FIG. 8j, ~~a~~ blanket delta layer 59 of electrically insulating material with the materials property of a high ratio of emitted secondary electrons when stimulated by a primary electron beam of sufficient energy is deposited to a thickness of 10 nm over the uncovered portions of gate dielectric layers 58, source electrodes 53, drain electrodes 54, and second isolation dielectric 56. A preferred material for delta layer 59 is magnesium oxide deposited by vacuum evaporation.

Amend paragraph 105 as follows:

As shown in FIG. 8k, delta layer 59 is coated with a liquid polymer material, such as PI2610 supplied by HD Microsystems, and cured at 350°C to a preferred film thickness of 1 - 1.5 μm to form an electrically insulating layer 60. A blanket layer 61 of chromium is sputter deposited over delta layer 59 to a preferred thickness of 300 nm.

As shown in FIG. 8l, chromium layer 61 is coated with a positive tone photoresist 100 and exposed to actinic light through a photomask, with alignment and optical

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registration, ~~registration~~ to superimpose a pattern 109 over previously defined gate dielectric 58. Photoresist 100 is ~~layer 58, and~~ subsequently developed by conventional means to define pattern 109 in resist 100 whereby portions of chromium layer 61 are uncovered. The uncovered chromium is chemically etched in a commercially available etchant provided by Transene Chemicals or other vendor to remove chromium metal in the regions defined by pattern 109 to define collector grid 62, and to expose portions of insulating layer 60 in regions overlying gate dielectric 58.

The exposed regions of layer 60 are etched by RIE, using oxygen plus fluoride ion gas chemistry, to remove the portions of polymeric insulating layer 60 in the regions not protected by collector electrode 62 to form collector insulator 63. See ~~insulator 63 as shown in~~ FIG. 8m. Chromium has high selectivity to the etchant chemistry, and so provides a suitable etch mask for removal of polymer. Additionally, delta layer 59 is not attacked by this etchant chemistry, and so serves an etch stop to protect gate dielectric 58 from damage. Photoresist 100 having pattern 109 is removed. TFTs 204 of active matrix 201 are now complete.

Amend paragraph 106 as follows:

In order to construct a liquid-crystal spatial light modulator, display electrodes 31 and spacing elements 43 must be released from mandrel substrate 20. FIGs. 9a - 9d (collectively "FIG. 9") illustrate steps in accordance with the invention for removing mandrel substrate 20 in manufacturing the light modulator of FIG. 1a. ~~FIG. 1.~~ To improve handling properties during release, and provide a robust backing for the array during subsequent liquid-crystal cell processing, a sacrificial backing film is created. As shown in FIG. 9a, a layer of dry film photoresist 101 is laminated to TFT array 201, making contact only to collector grid 62, to a form sub-assembly 110. A preferred dry film photoresist is Riston Tentmaster dry film tenting resist formulated to span the space between features similar to collector grid 62. Resist 101 is laminated to collector grid 62 by a heated roller process at 105°C, following array processing. Riston is a negative tone photoresist, with polymerization in areas exposed to actinic light. In this case where Riston is used as a sacrificial film and must be

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subsequently removed, resist 101 is not exposed to actinic light in order to facilitate stripping of the protective Riston film material following the cell fabrication process.

Amend paragraph 107 as follows:

A single edge termination of laminated resist 101, overlying completed TFT active-matrix array 201 and including mandrel 20, is attached by an adhesive film strip 151 to a delamination roller 150 as shown in FIG. 9b. Roller 150, with rotation as shown in FIG. 9b, produces delamination of subassembly 110 from mandrel 20. The delamination of subassembly 110 from mandrel 20 takes place at the surface of mandrel 20 coated with mold release 22 to reveal the lower modulator surface ~~701~~ formed with spacing elements 43 and display electrodes 31 as shown in FIG. 9c.

Amend paragraph 108 as follows:

In order to obtain good optical characteristics, liquid-crystal cells 202 must possess ordered alignment of their liquid-crystal molecules. This is typically accomplished by depositing a thin dielectric layer (not shown) over the lower modulator ~~common electrode 91 and~~ array surface. ~~surface 701.~~ A preferred material is silicon oxide deposited over display electrodes 31 and associated spacer elements 43 to a thickness of 20 nm by vacuum evaporation means to form an alignment surface as shown in FIG. 9d.

Amend paragraph 109 as follows:

FIGs. 10 - 13 illustrate the remaining steps in accordance with the invention for manufacturing the light modulator of FIG. 1a After forming common transparent electrode 91 on transparent modulator substrate 90, ~~FIG. 1. Referring to FIG. 10,~~ thermoplastic resin seal material, such as UVG-21 supplied by Cardinal Industries, is dispensed over common electrode 91 in a pattern corresponding to the perimeter of subassembly 110 to form a perimeter seal ring 710. See FIG. 10. The width of perimeter seal 710 is 0.25 - 0.5 mm. A

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gap 711, typically 3 - 5 mm, in the perimeter seal pattern facilitates subsequent filling of the liquid-crystal material following cell assembly. A first cure of seal ring 710 is obtained by exposure of the uncured ring to actinic light at a wavelength of 240 - 365 nm.

Amend paragraph 111 as follows:

The liquid-crystal material for liquid-crystal cells 202 is introduced into the cavity formed by subassembly 110 and electrode 91 by way of seal ring gap 711 as shown in FIG. 12. After filling, sufficient pressure is applied to backing resist 101 to remove excess liquid-crystal material by expelling through gap 711. Flexible subassembly 110 conforms to the contour of electrode 91 overlying substrate 90 so that spacing elements 43 make contact to electrode 91 as shown in FIG. 13. Gap 711 is sealed by conventional means using UV-cured adhesive supplied by Norland Products.

Amend paragraph 112 as follows:

Resist 101, which has not been exposed to actinic light, is removed by spray developing in a Riston developer. Liquid-crystal cells 202 are hermetically sealed in the cavity formed by subassembly 110 and electrode 91, ~~in a cavity 71~~ and are protected from the spray developing solution. Exposed features 59, 62, and 63 are also not affected by spray developing.

Amend paragraph 120 as follows:

The present light modulator can be fabricated using compatible materials and manufacturing techniques other than those described above. Light passbands outside the visible passband can be modulated in accordance with the invention. Various modifications and applications may thus be made by those skilled in the art without departing from ~~form~~ the true scope of the invention as defined in the appended claims.

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